REMARKS

Reconsideration of this application is respectfully requested. Claims 3, 4, 12, 13, 15 and 20 have been previously canceled. As such, claims 1, 2, 5-11, 14 and 16-19 are in this application and are presented for the Examiner's consideration in view of the following additional comments in preparation for appeal.

Claims 1, 2, 6, 7, 14 and 16 have been rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent Publication 2003/0202541 published October 30, 2003 for Lim et al. (*Lim*) in view of U.S. Patent Publication 2003/0117979 published June 26, 2003 for Chitrapu (*Chitrapu*). Applicants respectfully still disagree.

Applicants offer the following comments with regard to the Examiner's response to Applicants' arguments. The Examiner states

> that the "number of frames to process" corresponds to the one or more frames detected by slot synchronization.
>
> Office Action, p.2.

Respectfully, the Examiner is still wrong in the characterization of *Lim*. First, frames are not detected by slot synchronization – they are detected by correlating to the SSCH codes. This is a technical fact. (Applicants' specification, p. 2, lns. 3-9.) In addition, first slot synchronization occurs by determining the slot timing. In other words, the received signal is searched for the primary synchronization channel to first achieve slot synchronization. Then, after slot synchronization, **new** frames are processed to achieve frame synchronization, i.e., where the frame starts. As such, processing during slot synchronization has nothing to do with the number of frames processed during frame synchronization. Indeed, *Lim* states:

> [t]he multistep cell search algorithm includes in the first-step a search, in the second-step a cell search and in the third-step another cell search. In the first-step cell search process, a UE receives primary synchronization channel (P-SCH) signals transmitted from a Node B and acquires slot timing for a signal received at the highest power among the received P-SCH signals. In the second-step cell search process, the UE acquires slot synchronization based on the slot timing information acquired in the first-step cell search process, and then acquires frame synchronization and

> detects a Node B group to which the UE belongs by receiving a secondary synchronization channel (S-SCH) transmitted from the Node B. In the third-step cell search process, the UE finally searches for its source Node B using a scrambling code for the Node B by receiving a CPICH signal transmitted from the Node B based on the frame synchronization and Node B group information acquired in the second-step cell search process.

Lim, paragraph [0011], emphasis added.

As noted above, *Lim* describes a multistep cell search algorithm. The first step is used to acquire slot timing. Then, the second step is used for frame synchronization. As such, and as stated earlier, the processing in the first step has nothing to do with the number of frames processed in the second step.

Second, FIG. 1 of *Lim* is simply used to show the structure of a single frame. (*Lim*, paragraph [0013]) FIG. 1 of *Lim* does not show the slot synchronization and frame synchronization.

Third, the Examiner's characterization of Applicants specification is wrong. The Examiner quotes Applicants' specification, paragraph 7, as follows:

> [p]erforms frame synchronization using a received second synchronization channel in such a way that the received first synchronization channel is now used by the wireless receiver to adjust for frequency offset. Thus, the effect of frequency offset on the process of frame synchronization is reduced, if not eliminated.
>
> Office Action, p. 3; emphasis added.

Yet – not only is this NOT paragraph 7, of Applicants' specification, - NOWHERE is this text found in Applicants' specification. As such, it would appear that the Examiner's use of this text is improper. In addition, the Examiner's conclusion based on this wrong citation is also in error. In particular, the Examiner then states that "[f]rame synchronization occurs by determination of a frequency offset obtained from the slot synchronization". Respectfully, this is wrong. In particular, the wrongfully cited text does not state that frame synchronization occurs by determining frequency offset – the wrongfully cited text states that "the effect of frequency offset on the process of frame synchronization is reduced, if not eliminated". Reducing the effect of

frequency offset on the process of frame synchronization is not the same as determining frequency synchronization.

Similar comments apply to the Examiner's reference to paragraph [0019], of Applicants' specification. The Examiner's cited text simply DOES NOT EXIST anywhere in Applicants' specification. As such, it would again appear that the Examiner's use of this additional text is improper.

For all the above reasons, the Examiner's response to Applicants' arguments is flawed.

Turning now to Applicants' previous arguments in Applicants' previous response, the combination of *Lim* and *Chitrapu* does not yield Applicants' claimed invention. The plain language of Applicants' independent claims 1 and 14 is clear. A peak correlation value is associated with the first synchronization value (slot synchronization). This peak correlation value is then used to determine a number. This number is the number of frames to process the second synchronization channel to acquire **frame synchronization**.

The Examiner's cited portions of *Lim* simply refer to correlation values and acquiring slot synchronization. There is no description in *Lim* that a correlation value from the slot synchronization is used to determine a number as claimed by Applicants. Indeed, *Lim* simply states that:

> [t]herefore, it is possible to acquire information on a code group, i.e., a Node B group, where the UE belongs, and information on frame synchronization by receiving a secondary synchronization channel signal for a period of several time slots, correlating secondary synchronization codes with a secondary channel signal for the period of several time slots, and performing a cyclic shift operation on each of the 64 codewords 15 times. The term "frame synchronization" means synchronization on timing or phase within one period of a scrambling spreading code for a spread spectrum system. In the existing W-CDMA mobile communication system, one period of a spreading code

> and a length of a frame are both 10 ms, so this is called "frame synchronization."
>
> *Lim*, paragraph [0015], emphasis added.

Nowhere does the above-cited portion of *Lim* describe that a number was derived from the slot synchronization for determining the number of frames for acquiring frame synchronization as claimed by Applicants. *Lim* simply describes to use a period of several time slots for frame synchronization. There is no description, or suggestion, in *Lim* of determining a number to use during frame synchronization as a function of a correlation value from slot synchronization as claimed by Applicants.

Similar comments apply to *Chitrapu*. Indeed, *Chitrapu* states:

> The results of the SSC correlations for each frame are accumulated until a confidence level is determined using a rule based approach, (74). Factors considered in the confidence level determination are the received magnitude and shape factor of each SSC, the variation in each received SSCs magnitude and shape between frames and the allowed SSC combinations. Additionally, information from previous successful cell synchronizations may be included, (75). The previous information may contain the previously detected SSCs at a given frame location. If SSC codes are detected at a location associated with a prior successful synchronization, the confidence in the SSC detection is increased.
>
> *Chitrapu*, paragraph [0048], emphasis added.

Again, nowhere does the above-cited portion of *Chitrapu* describe that a number was derived from the slot synchronization for determining the number of frames for acquiring frame synchronization as claimed by Applicants. *Chitrapu* simply describes to accumulate correlations until a confidence limit is reached. There is no description, or suggestion, in *Chitrapu* of determining a number to use during frame synchronization as a function of a correlation value from slot synchronization as claimed by Applicants.

In view of the above, Applicants respectfully submit that independent claims 1 and 14 are patentable over *Lim* in view of *Chitrapu*. As such, dependent claims 2, 6, 7 and 16 are also in condition for allowance.

Claims 5 and 8 have been rejected under 35 U.S.C. §103(a) as being unpatentable over *Lim* in view of *Chitrapu* and further in view of U.S. Patent Publication 2003/0045299 published March 6, 2003 for New (*New*). Applicants respectfully traverse for the reasons described above with respect to independent claim 1.

Claims 9-11 and 17-19 have been rejected under 35 U.S.C. §103(a) as being unpatentable over *Lim* in view of *Chitrapu* and further in view of U.S. Patent Publication 2004/0161020 published August 19, 2004 for Mathew et al. (*Mathew*). Applicants respectfully traverse for the reasons described above with respect to independent claims 1 and 14.

As it is believed that all of the objections set forth in the Official Action have been fully met, favorable reconsideration and allowance are earnestly solicited. If, however, for any reason the Examiner does not believe that such action can be taken at this time, it is respectfully requested that the Examiner telephone Applicants' attorney in order to overcome any additional objections that the Examiner might have.

If there are any additional charges in connection with this requested amendment, the Examiner is authorized to charge Deposit Account No. 07-0832 therefor.

Respectfully submitted
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